PheniX-Volga: Germanium Double Sided Strip Detector development program at IRAP

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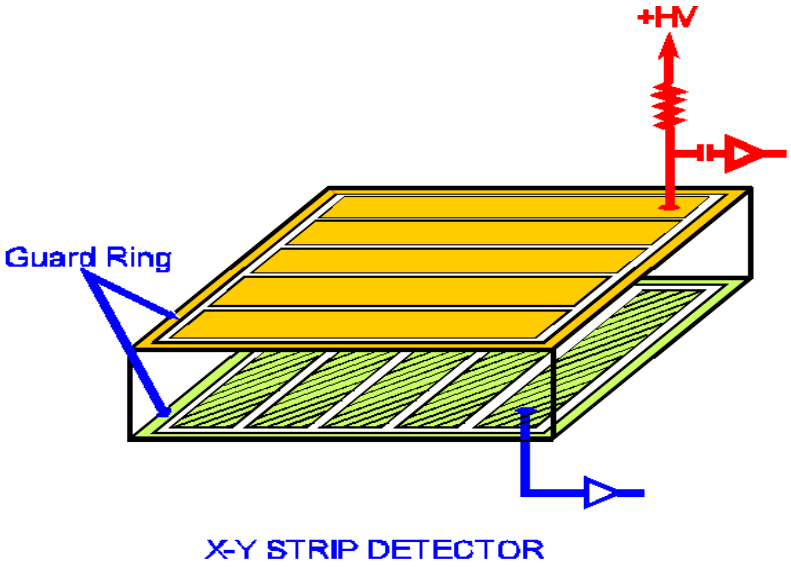
(On behalf of Phenix-Volga's team)

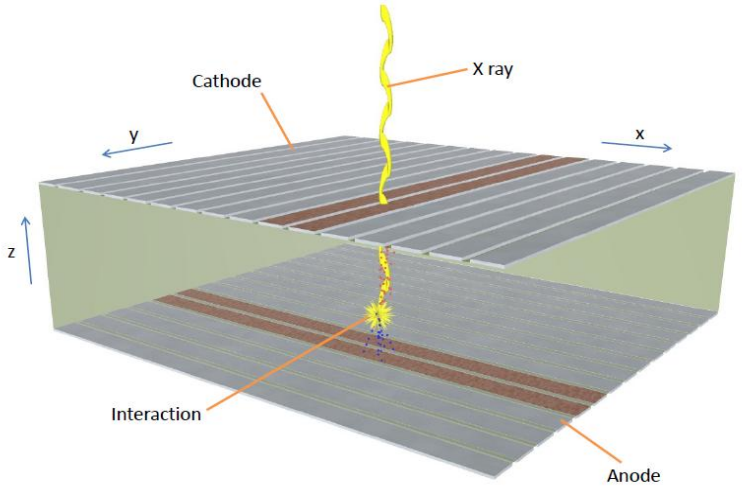
Main goals

- To study a new generation of detector, intended to be placed at the focal point of a hard X-ray telescope
  - high energy and spatial resolution
  - broad X-ray coverage up to 200 keV
  - 3D localization capabilities
- To achieve a good level of qualification and Test Readiness of the detection system (space context)

Germanium DSSD

- High purity Germanium HPGe diode
- Planar Double Sided Strip Detector (DSSD)
  - 3D spatial localization of the photon interaction
  - N*N pixels with only 2*N electronic channels





Roadmap of the Ge DDSD at IRAP

- The Ge DSSD was initially part of the PheniX proposal, submitted to ESA for its mission M3 in 2010, but not selected.
- R&T phase 1 program, funded by CNES (sept 2011 – dec 2012)
- R&T phase 2 program, funded by CNES (jan 2013 – april 2014)
- *3rd R&T program, submitted to CNES (answer january 2014)*
- *Future work : full detector demonstrator (> 2015)*

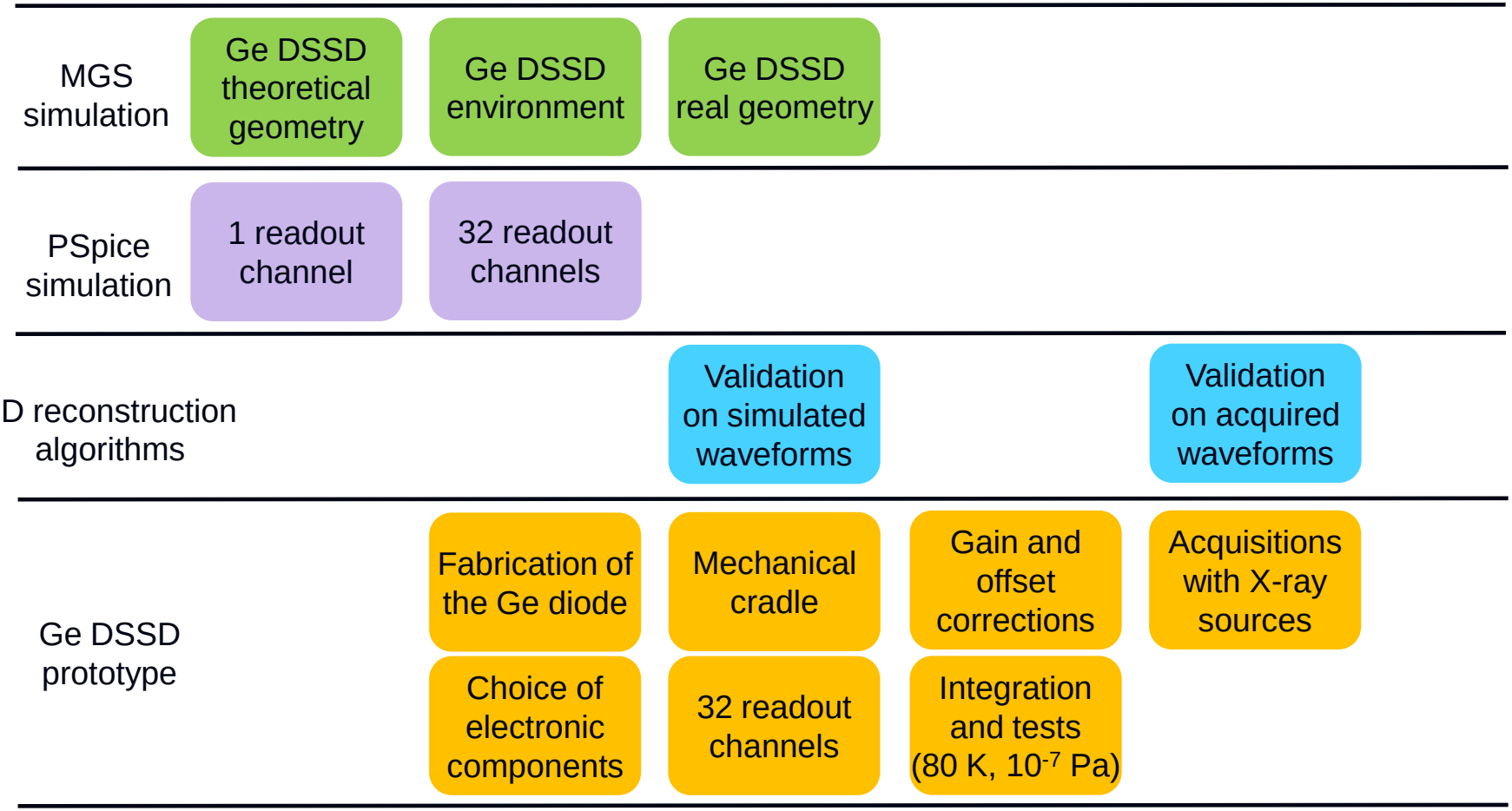
R&T phase 1: objectives

- Main objectives:
  - Improve our understanding of the Ge DSSD
  - Achieve a 3D digital reconstruction of the photon interactions
  - Design a whole detection system with a Ge DSSD

- Developments:
  - Simulation of the Ge DSSD response *(presentation of Isidre Mateu)*
  - Simulation of the analog electronic chain
  - 3D reconstruction algorithms *(presentation of Isidre Mateu)*
  - Ge DSSD prototype with 32 (16*2) electronic channels

R&T phase 1: roadmap

- R&T phase 1: sequence of actions

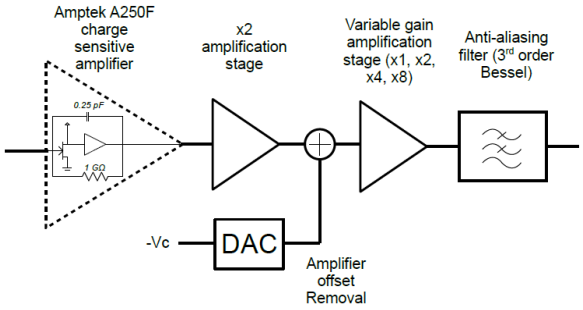


R&T phase 1: simulations

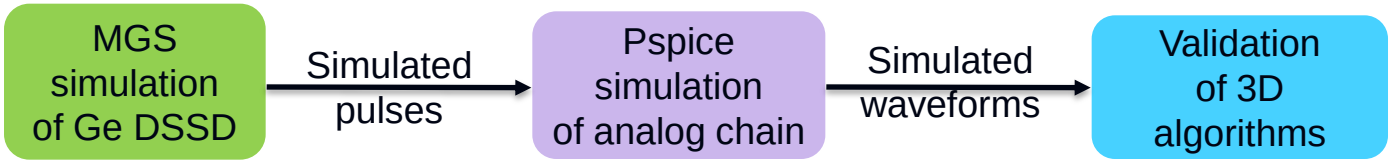
- Simulation of the Ge DSSD with MGS software
  - *(see next presentation of Isidre Mateu)*
  - Provides good knowledge of the diode and its context
    - the geometry of the strips
    - the influence of the metal parts of the cradle on the Diode
    - the guard ring properties
  - The simulated pulses generated by MGS have been used as inputs for the analog electronic chain simulation

R&T phase 1: 3D algorithms

- Validation of 3D algorithms on simulated data
  - The analog chain has been simulated with an Amptek A250F charge sensitive amplifier (A250 + JFET)



  - The simulated waveforms have been used as inputs for 3D algorithms until the Ge DSSD prototype is finished



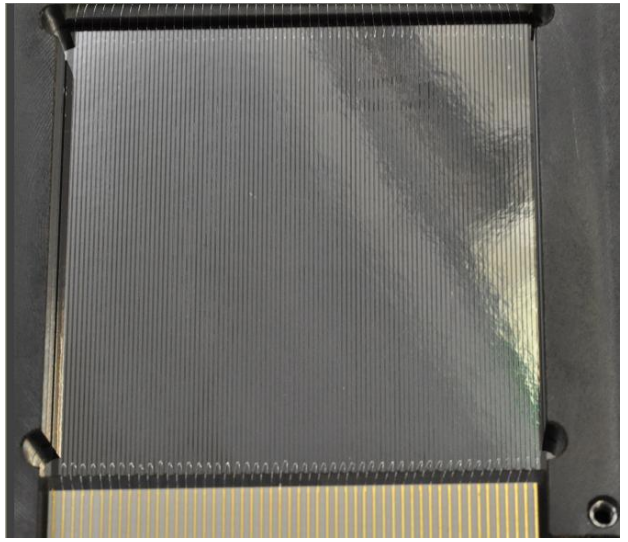
R&T phase 1: prototype (roadmap)

- Development of a Ge DSSD prototype with 32 channels
  - Processing of the 100X-100Y Ge diode
  - Mechanical integration of the diode
  - Qualification of the Ge diode process
  - Development of 32 electronic channels
  - Integration in the cryostat

R&T phase 1: prototype (Ge diode)

- Processing of the 100X-100Y Ge diode by Canberra (Lingolshein, France)
  - 100X-100Y, 350 µm wide strips, gap of 50 µm
  - 50 even strips, 50 odd strips for one face, same for the perpendical strips of the back face

Cristal: 51x51 mm, thickness = 11.7 mm
Detection area: 40x40 mm

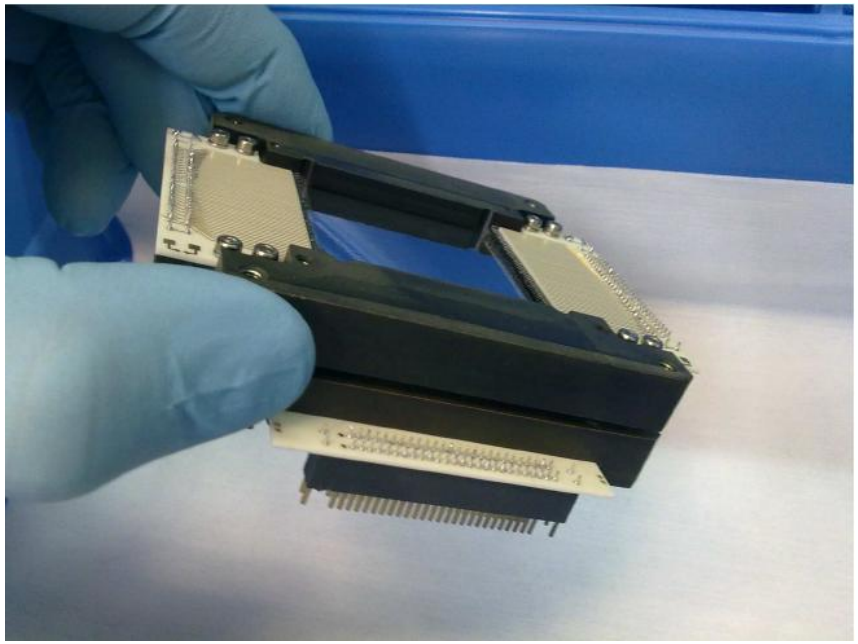


Bondings of 50 strips in one PCB

R&T phase 1: prototype (Ge diode)

- Mechanical integration of the diode
  - Choice of a cradle prototype in Vespel, good insulator, non metallic, not intended to pass vibration tests
  - use of 64 pins qualified connectors (Omnetics)

Material : Vespel
XY plane = 75x75 mm
Thickness = 35 mm



R&T phase 1: prototype (Ge diode)

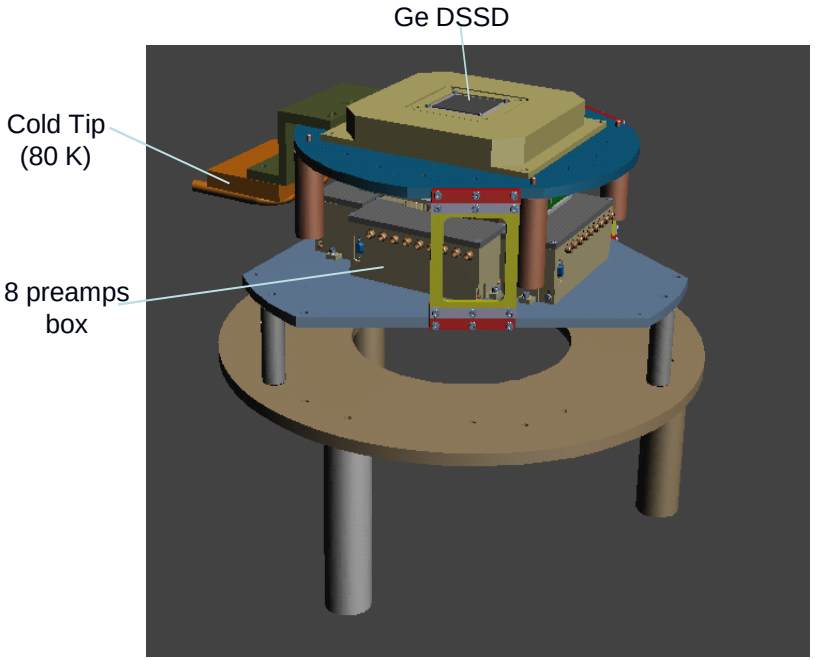
- Qualification of the Ge diode fabrication process
  - 30 thermal cycles (-200°C - +80°C)
  - Several openings of the cryostat (air)
  - Leakage current OK
  - Tension of depletion of 1700 V
  - *2 complete disassembly to repare the bondings*

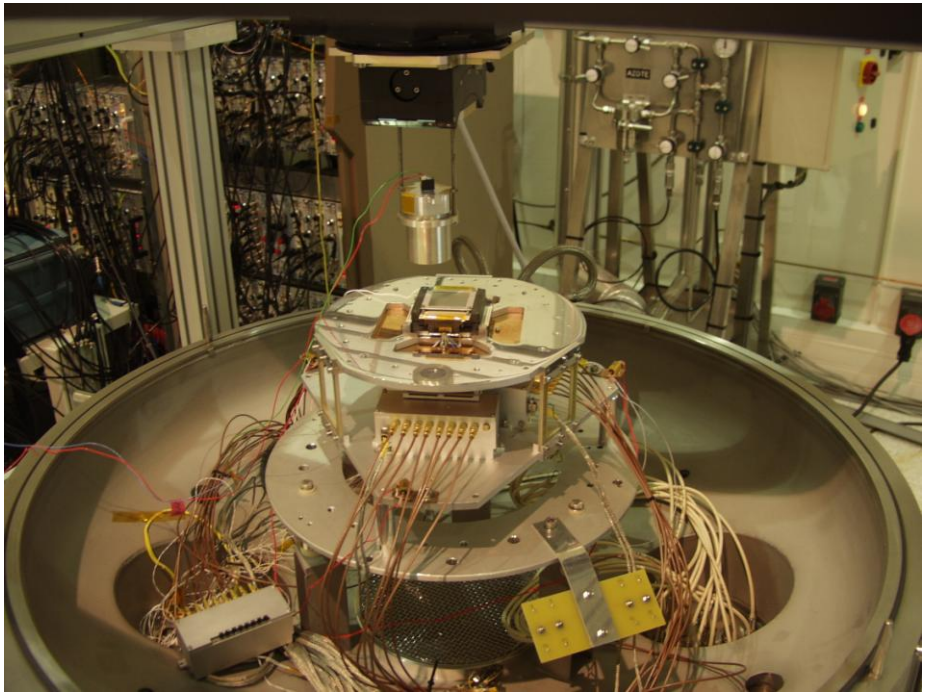
R&T phase 1: prototype (electronics)

- Development of the 32 electronic channels
  - Choice of the Amptek A250F charge sensitive amplifier (A250 + JFET)
    - A250 already qualified for ESA
    - Less noise if the A250F is cooled (0.7 keV at -80°C)
  - Choice of an early digitization of the signal
    - The gain and correction offset stages are located outside the cryostat (David Murat, IRAP)
    - The ADC stage is provided by a COTS 32 channels digitizer (N6740, 62.5 MHz, CAEN, Italy)
    - The waveforms provided by the digitizer are analysed offline by the 3D reconstruction algorithms

R&T phase 1: prototype (integration)

- Integration of the Ge DSSD and the 32 electronic channels into the cryostat of SPI Integral, at IRAP
  - Ge DSSD : 103 K, 3.10^{-7} mbar





R&T phase 1: conclusions

- Phase 1 : conclusions
  - Validation of Ge DSSD and electronic chain simulations
  - Validation of the 3D algorithms on simulated data
  - Qualification of the Ge diode process
  - Half qualification of the front-end electronic chain
    - Connectics OK, A250 OK, JFET to be done
  - *The diode cradle can not pass vibration tests*
  - *The electronic chain has to be improved*

➔**R&T phase 2 accepted by CNES, started on january 2013**

R&T phase 2: objectives

- Main objectives:
  - Validate the 3D algorithms on real data (first prototype)
  - Increase the Test Readiness Level (TRL) of the detector system
  - Reduce the noise of the electronic chain
  - Increase the detection area of the Ge DSSD

- Developments:
  - Calibration algorithms
  - STM to pass the vibrations tests specified by ESA
  - Discrete preamplifiers with cold JFET
  - Transition from 32 to 128 electronic channels

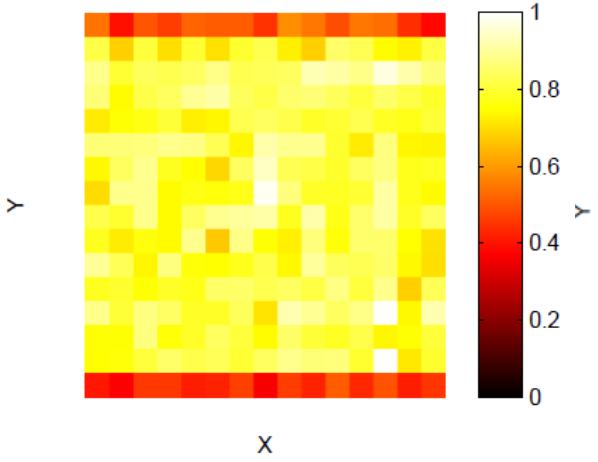
R&T phase 2: roadmap

- R&T phase 2: sequence of actions

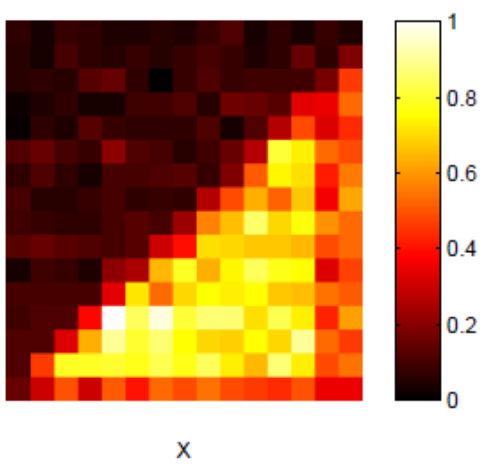
Ge DSSD prototype 32 channels	Acquisitions with X-ray sources	Tests of a single PA with cold JFET		Ge DSSD prototype 128 channels	Acquisitions with X-ray sources
3D algorithms	Calibration algorithms	3D reconstruction on real data			
STM	Mechanical cradle in Titanium diode in steel	Vibration Tests	Scaling factor for the new cradle of Ge DSSD		
128 channels	Discrete PA optimization	Discrete PA with cold JFET (prototype)	128 discrete PA with cold JFET		

R&T phase 2: 3D algorithms validation

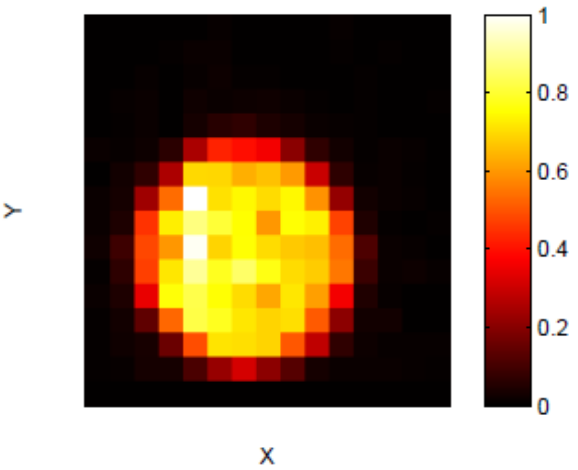
- Validation of 3D algorithms
  - Use of the Ge DSSD prototype with 32 channels
  - 16*2 channels = 16*16 (256) pixels of 350 µm
  - Results in next presentation of I.Mateu



uniform irradiation ^{241}Am



iron mask 45° ^{241}Am

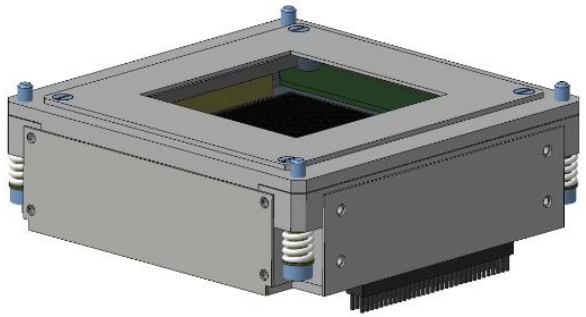


tungsten collimator ° ^{241}Am

R&T phase 2: STM and vibration tests

- STM of the detector assembly
  - Cradle in Titanium, for its thermal conductivity and sturdiness
  - Fake diode in steel of 90x90x15 mm, same size as a detector in a space telescope
  - Mechanical clamping only on the 2 faces, 90 DaN to the diode
  - Vibration levels recommended by ECSS for a spatial prototype
    - rdr = 0,5 g
    - sine 3 axes = 20 g
    - random X = 24,32 g r.m.s.
    - randomY,Z = 15,69 g r.m.s.

➔ **Tests passed successfully**

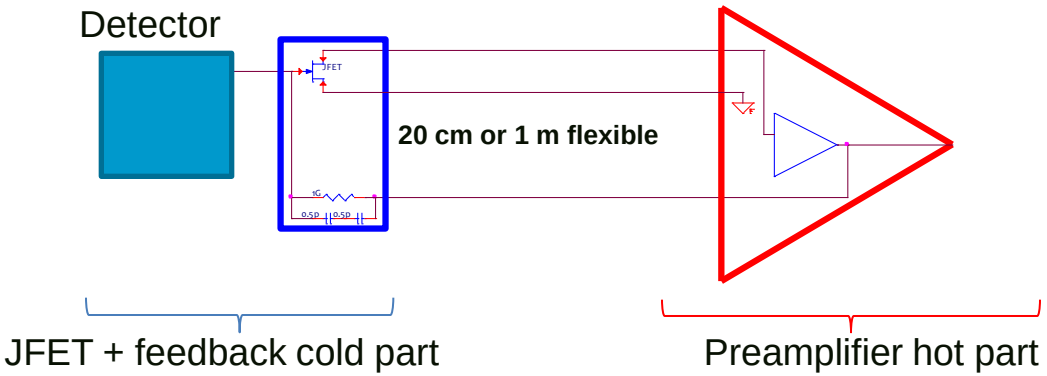


78 x 78 x 23 mm

  - Scaling factor for the design of the functional Ge DSSD cradle

R&T phase 2: electronics

- New design for the 128 electronic channels
  - Choice of a discrete preamplifier (high cost of A250)
  - Choice of a PA with separated JFET



R&T phase 2: electronics

- Advantages to separate the JFET from the PA
  - Shortening the JFET - detector connection (less noise)
  - Increasing the JFET - PA connection (up to 1 meter)
    - Outside the anti coincidence shielding
  - Cooling the JFET to decrease the noise becomes possible
  - No need to cool the PA at -80°C, use of a flexible connection

    ➔JFET (130 K) and PA (25°C): < 0.2 keV expected

- Drawbacks
  - JFETs consume more cold power
  - The capacitors near to the JFET must also be cooled on the High Voltage side

R&T phase 2: integration of 128 channels

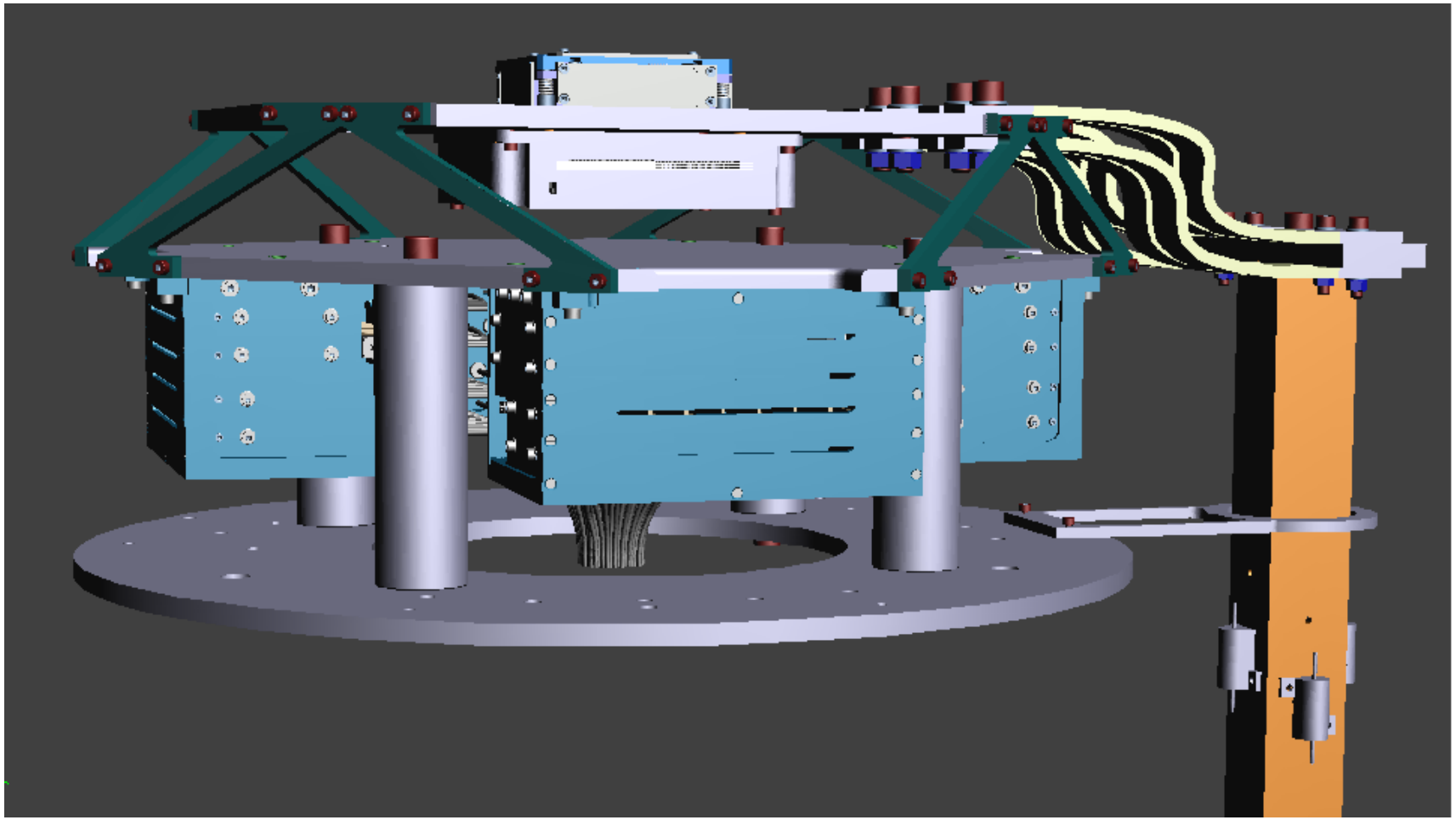
- Transition from 32 to 128 channels
  - Reduction of the cost of the components
  - Cooling power improvement, thermal leakage reduction
  - Miniaturization to optimize the available space

PT cryocooler

32 Preamplifiers in one box

R&T phase 2: integration of 128 channels

- Assembly for the Ge DSSD 128 channels (64*64 pixels)



R&T phase 2: conclusions

- Phase 2 : conclusions
  - TRL 4.5 reached on the detector mechanical assembly
  - Detection area increased up to 25*25 mm (64*64 pixels)
  - Low-noise electronic chain with cold JFET

  - *Thermal validation of the detector system to be done*
  - *Qualification of the analog electronic chain to be done*
  - *Minimal size with discrete components already reached*

➔**R&T phase 3 submitted to CNES**

R&T phase 3: objectives

- Main objectives:
  - Characterization of the Ge DSSD with 128 channels working prototype
  - Reduction of the mass and power budget of the detector assembly

- Developments:
  - Hybridation of 128 PA components
  - Hybridation of 32 cold JFETs

➔**Selection of the R&T program phase 3 end of january 2014**

Future work: > feb 2015

- Main objectives:
  - Production of a full detector demonstrator (200*200 pixels)

- Developments:
  - Integration of the triggers, gain, correction offset into FPGAs
  - Integration of the 3D reconstruction algorithms into DSPs

➔**Fundings to be found**